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Original Article

IMPACTS OF VARIATIONS IN CHANNEL LENGTH, WIDTH AND GATE WORK FUNCTION OF GAN FINFET AND SI-FINFETON ESSENTIAL ELECTRICAL PARAMETERS

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ABSTRACT

Recently, III–V compound material-based channels are being seriously considered as a credible alternative candidate than conventional silicon-(Si)-based channel for designing robust nanodevices. III - V FinFETs have high carrier mobility and less short channel effect (SCE) than Si transistors. In this paper, the impacts of variations of channel lengths (8 and 10 nm) and channel widths (10 and 12 nm) on electrical parameters, such as mobility, drain-induced barrier lowering (DIBL), gate capacitance and gate work function of double gate n-channel gallium nitride (GaN), FinFET and Si-FinFET and finally, variation of gate work function on threshold voltage of both FinFET shaves have been carefully observed. A comparative study for both FinFET structures have been presented to find out valuable findings. Extensive experimental evaluations for different parameters validate the superiority of GaNFinFET compared to Si-FinFET. The self-consistent solutions of Poisson, Drift Diffusion and Fermi level equations have been used to demonstrate detailed simulation results. For precise calculations, the multigate FET (MuGFET) tool of nanoHUB.org which uses PADRE simulator has been used. Finally, for better simulation results, Origin Lab simulator has also been employed. For better electrical performances of 8-nm channel length as well as gate length and 10 nm channel width of GaN FinFET than Si-FinFET must be considered to design future nanodevices.

KEYWORDS: GaNFinFET, Si-FinFET, Channel Length, Channel Width & Gate Work Function

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1. INTRODUCTION

For finding better heterojunction III–V material-based channel, we have employed GaN channel to compare several electrical parameters such as mobility, DIBL, gate capacitance and gate work function with single material-based channel like silicon. We have observed that GaN channel is more effective than Si channel. The GaN has wideband gap of 3.4 ev, which illustrates its special properties for applications in optoelectronic high-power and high-frequency devices[1-3]. Moreover, we have observed that the GaN is a better channel material than silicon due to its mechanically fixed wide band gap with high heat capacity and thermal conductivity[4]. It has shown that GaN has credible stability in radiation environments for military and space applications[5]. The GaN attains remarkable encouraging characteristics for GHz/THz devices[6-8]. Enhancement mode of GaN transistors became generally obtainable in 2010[9]. GaN has very high breakdown voltages, high electron mobility and saturation velocity that made it an ideal candidate for high-power and high-temperature microwave applications[10,11]. The GaN can be

doped with silicon (Si) or with oxygen to n-type and with magnesium (Mg) to p-type for this GaN crystals introduce tensile pressure making them frail[12,13]. An issue of concern scaled in more heterojunction like In GaAs FinFET is the strong dependence of electrical parameters such as threshold voltage and leakage current on Fin width as a consequence of quantum confinement effects[14]. The excess off-state current in tight-pitch In GaAs QW-MOSFET is strongly gate length dependent, making it highly problematic in nanoscale devices and also affected by certain mismatch problems[15].

We have carefully demonstrated the impacts of variation of channel lengths (8 and 10 nm) and channel widths (10 and 12 nm) on electrical parameters, such as mobility, drain-induced barrier lowering (DIBL), gate capacitance and gate work function of double gate n-channel GaN FinFET and Si-FinFET and finally, variation of gate work function on threshold voltage of both FinFETs. The paper is organized as follows:

Section 2 deals with device structure and dimensions; Sec. 3 illustrates methods; Sec. 4 reviews results and discussions. Finally, Sec. 5 summarizes the whole research work as conclusion.

2. DEVICE STRUCTURE AND DIMEMSIONS

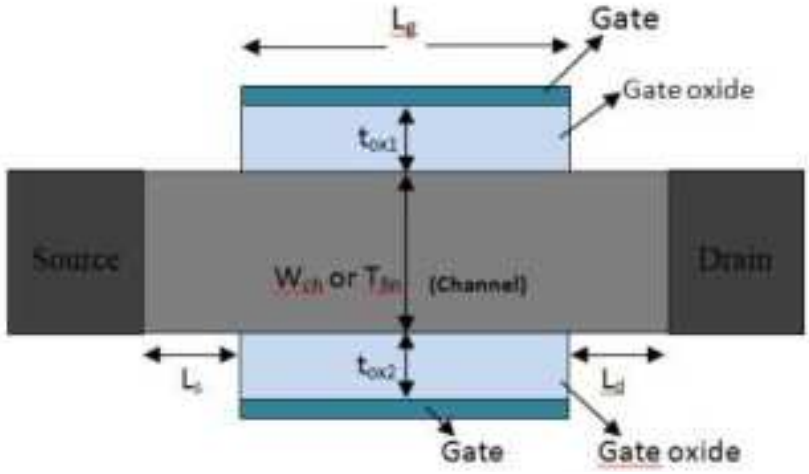

Figure 1: Two dimensional Dougle-Gate FinFET[16].

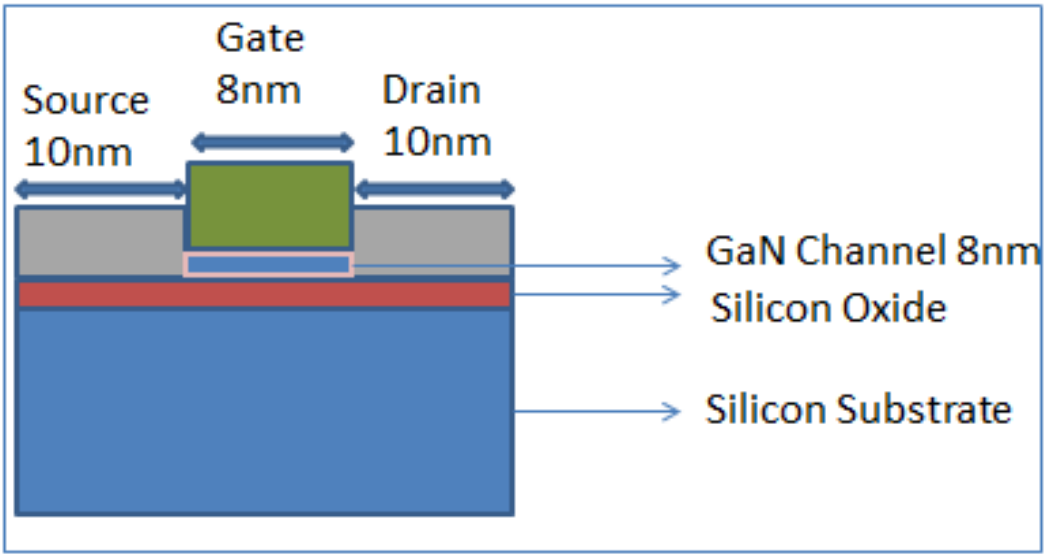

Figure 2: Nanostructure of GaN used as Channel Material.

The device structure of double gate n-channel FinFET structure has been depicted in Figure 1. In figure. 1, gate length also called channel length indicated by L_g and channel width W_{ch}. An oxide layer is placed on either side of the channel and also at the top surface of the channel. The thicknesses of the side wall oxide are denoted by T_{ox1} and T_{ox2} [16]. Figure 2, a simple nanostructure of GaN material-based channel has been displayed. For our simulation work, we have used 2 nm thickness for oxide layer, 10 nm thickness of channel width, 8-nm gate length as well as channel length and 10 nm for both source and drain extension lengths. The drain/source doping has been kept fixed at 1 x 10^{20} cm^3 and channel 1 x 10^{16} cm^3. Gate bias has been taken from 0 V to 1 V, drain bias varied from 0 V to 1.2 V, gate length varied from 0 μm to 0.1 μm and gate work function varied from 0 ev to 1 ev. We have chosen different physical constants and related parameters for different materials[17].

3. METHODS

To study different characteristic variations, we have used MuGFET tool provided by nanoHUB.org, which uses drift-diffusion type simulator PROPHET and PADRE. The PROPHET and PADRE are self-consistent simulators. PROPHET can solve Poisson and Drift Diffusion equations and PADRE can solve Fermi level equations. For our better simulation results, PADRE simulator has been used. The NanoHUB.org is online-based simulator software, which is widely used to find accurate simulation results. FinFET technology based on the values of oxide layer thickness, thickness of channel width, gate length as well as channel length, both source and drain extension lengths and other related parameters. For accurate result, at first, we have collected the approximate data for the material that is used as channel. Then the different related values of parameters have been inputted into blank fields of the simulator. After simulation process, we have collected the extracted data from the simulator connected to online and then the extracted data also included into the Origin Lab simulator. Then the Origin Lab simulator has demonstrated the related comparative characteristic curves. Finally, the comparative characteristic curves have been designed perfectly.

4. RESULTS AND DISCUSSIONS

4.1 Impacts of Variations of Channel Length

4.1.1 Comparison of gate capacitance between GaNFinFET and Si-FinFET using 8 nm and 10 nm channel Length

Table 1: Variation of Gate Capacitance with respect to Gate Voltage for GaNFinFET and Si-FinFET using 8 and 10-nm channel Lengths.

Gate Voltage (V)	Gate Capacitance (fF)	Gate Capacitance (fF)	Gate Capacitance (fF)	Gate Capacitance (fF)
	Gate Capacitance of 10 nm channel length of GaNF in FET	Gate Capacitance of 10 nm channel length of Si-Fin FET	Gate Capacitance of 8 nm channel length of GaNF in FET	Gate Capacitance of 8 nm channel length of Si-Fin FET
0	0	0	0	0
0.2	2.94356	2.01433	3.1091	2.0541
0.4	5.87653	3.54201	5.98202	3.98012
0.6	6.78593	5.78201	6.9	6.30231
0.8	8.94568	7.41085	9.01784	7.92315
1	10.12349	9.9823	10.20317	10.10317

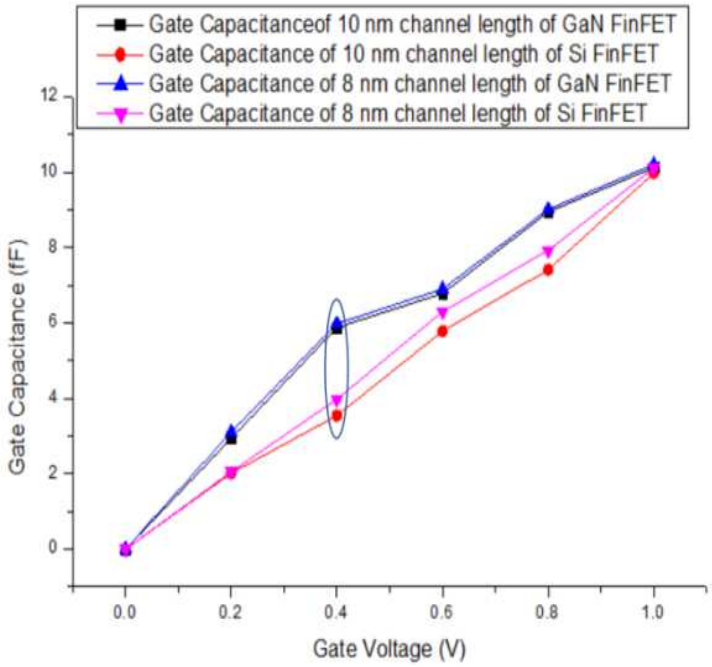

Figure 3: Comparison of Gate Capacitance between GaNF in FET and Si-FinFET using 8 and 10-nm Channel Lengths.

The compound material of GaN is widely used to design robust nanodevices. The gate capacitances strongly depended on threshold voltage. Higher the gate capacitance, lesser the threshold voltage. As the threshold voltage decreases, leakage current increases. From Figure 3, we have observed that at the same gate voltage, (0.4 V) gate capacitance is increased when channel length is decreased from 10 nm to 8 nm for both GaN FinFET and Si-FinFET. It is also observed that gate capacitance as well as leakage current is increased more for 8-nm channel length of GaN FinFET rather than 8-nm channel length of Si-FinFET. From this observation point of view, the electrical property of gate capacitance for Si-FinFET with respect to channel length is better than GaN FinFET transistor.

4.1.2 Comparison of Mobility between GaN FinFET and Si-FinFET using 8 and 10-nm Channel Lengths

Table 2: Variation of Mobility with respect to Drain Voltage for GaNFinFET and Si-FinFET using 8 and 10-nm Channel Lengths.

Drain Voltage(V)	Mobility(cm^2/Vs)	Mobility(cm^2/Vs)	Mobility(cm^2/Vs)	Mobility(cm^2/Vs)
	Mobility of 10 nm channel Length of GaNFinFET	Mobility of 10 nm channel Length of Si-FinFET	Mobility of 8 nm channel Length of Si-FinFET	Mobility of 8 nm channel Length of GaNFinFET
0	0	0	0	0
0.2	9.1234E-11	8.3871E-11	8.7601E-11	9.4108E-11
0.4	1.13524E-10	1.0021E-10	1.05781E-10	1.1592E-10
0.6	1.2543E-10	1.12654E-10	1.2E-10	1.2693E-10
0.8	1.37124E-10	1.31093E-10	1.32093E-10	1.4E-10
1	1.45623E-10	1.4012E-10	1.41E-10	1.47219E-10
1.2	1.53241E-10	1.48265E-10	1.5E-10	1.54E-10

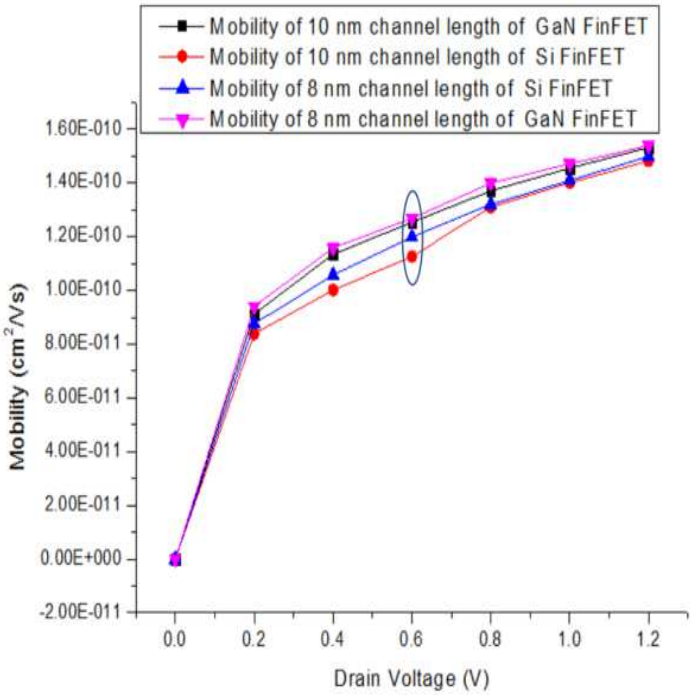

Figure 4: Comparison of Mobility between GaN and Si-FinFET using 8 and 10-nm Channel Lengths.

The mobility is proportional to electric potential, conductivity and trans conductance. As a result, more drain current (on current) is generated from the device. Almost always higher mobility leads to better device performance. In the depicted Figure 4, we have shown that we increase the drain voltage mobility for both Si-FinFET and GaNFinFET increases. Moreover, at the same drain voltage (0.6V), mobility is increased more when channel length is decreased from 10 nm to 8 nm for both GaN FinFET and Si-FinFET. It is also shown that mobility as well as electron drift velocity is increased more for 8-nm channel length of GaN FinFET rather than 8-nm channel length of Si-FinFET. From this observation point of view, we have decided that more reduced channel length of GaN FinFET is better than Si-FinFET.

4.1.3 Comparison of DIBL between GaNFinFET and Si-FinFET using 8 and 10-nm channel Lengths

Table 3: Variation of DIBL with respect to Gate Voltage for GaNFinFET and Si-FinFET using 8 and 10-nm Channel Length

Gate Voltage(V)	DIBL(mV/V)	DIBL(mV/V)	DIBL(mV/V)	DIBL(mV/V)
	DIBL of 10 nm Channel Length of GaNFinFET	DIBL of 10 nm Channel Length of Si-FinFET	DIBL of 8 nm Channel Length of GaNFinFET	DIBL of 8 nm Channel Length of Si-FinFET
0	0.11231	0.14236	0.10351	0.13902
0.2	0.13245	0.16431	0.12532	0.1528
0.4	0.15713	0.17316	0.14329	0.16342
0.6	0.17351	0.18256	0.1701	0.17469
0.8	0.18452	0.18921	0.17905	0.18431
1	0.19564	0.19561	0.18903	0.194

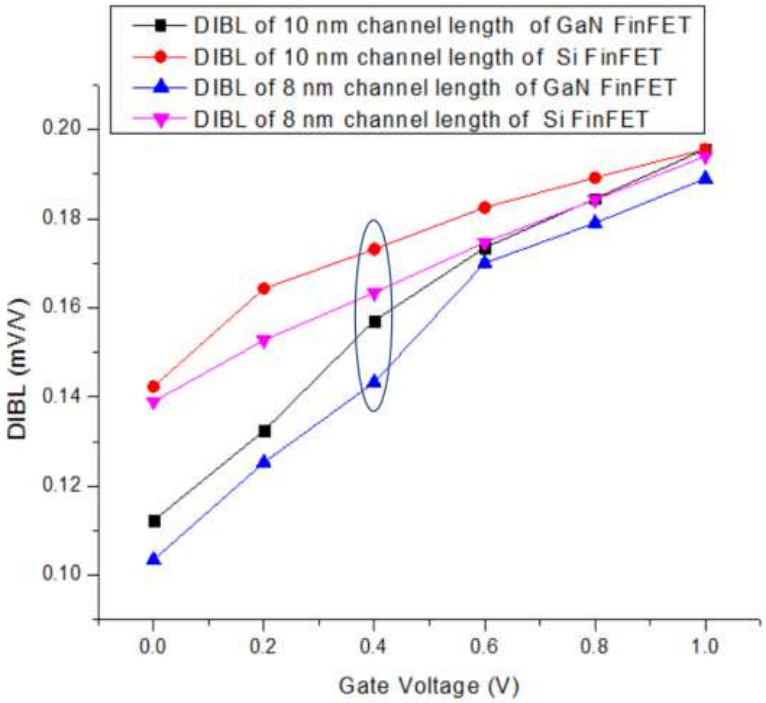

Figure 5: Comparison of DIBL between GaNFinFET and Si-FinFET using 8 and 10-nm Channel Lengths.

In FinFET device, as DIBL increases, drain current increases, but voltage threshold decreases, as a result current leakage from the device increases. For low-power nanodevices, lower DIBL is considerable. The reduced DIBL can improve threshold voltage roll-off property, maintained properly device operating frequency and also minimized short channel effect (SCE). In Figure 5, we have presented that if we increase the gate voltage, DIBL for both Si-FinFET and GaNFinFET increases. Moreover, at the same gate voltage (0.4 V), DIBL is decreased more when channel length is decreased from 10 nm to 8 nm for both GaN FinFET and Si-FinFET. It is also observed that DIBL is decreased more for 8-nm channel length of GaN FinFET rather than 8-nm channel length of Si-FinFET. From this observation point of view, we have considered that a more reduced channel length of GaN FinFET is better than Si-FinFET to design high-performance nanometer scale FinFETs.

4.1.4 Comparison of Gate Work Function between GaNFinFET and Si-FinFET

Table 4: Variation of Gate Work Function with respect to gate Length for GaNFinFET and Si-FinFET using 8 and 10-nm Channel Lengths

Gate Length(μm)	Gate Work Function(eV)	Gate Work Function(eV)	Gate Work Function(eV)	Gate Work Function(eV)
	Gate Work Function of 8 nm Channel Length of GaNFinFET	Gate Work Function of 8 nm Channel Length of Si-FinFET	Gate Work Function of 10 nm Channel Length of Si-FinFET	Gate Work Function of 10 nm Channel Length of GaNFinFET
0	1.1519	1.1301	1.1	1.14532
0.02	1.17917	1.13521	1.13278	1.17812
0.04	1.23	1.1831	1.1721	1.21563
0.06	1.27102	1.25231	1.193	1.26981
0.08	1.351	1.29511	1.27234	1.32621
0.1	1.45	1.37121	1.3251	1.4391

The gate work function (GWF) is the minimum energy needed to remove an electron immediately from solid surface to the outside of the solid surface. The GWF modulates energy bands of semiconductor devices. Higher GWF bends energy band upwards. As GWF increases, threshold voltage increases, but on current, transconductance as well as conductivity decreases. As a consequence, lower GWF is required for n channel FinFETs. In Figure 6, we have noticed that if we increase the gate length, GWF for both Si-FinFET and GaN FinFET increases. Further, at the same gate length, (0.04 μm) GWF is increased when channel length is decreased from 10 nm to 8 nm for both GaN FinFET and Si-FinFET. It is also observed that GWF is increased more for 8 nm channel length of GaN FinFET rather than 8-nm channel length of Si-FinFET. From this valuable observation, we have mentioned that the electrical property of GWF for Si-FinFET is better than GaN FinFET transistor.

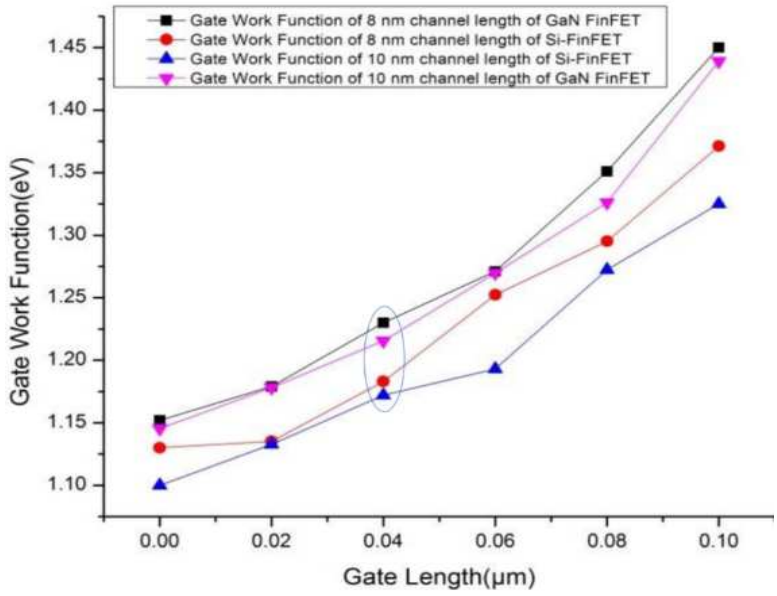

Figure 6: Comparison of Gate Work Function between GaN and Si-FinFET using 8 and 10-nm channel Lengths.

4.2 Impacts of Variations of Channel Width

4.2.1 Comparison of gate Capacitance between GaNFinFET and Si-FinFET using 10 and 12-nm Channel Widths

Table 5: Variation of gate Capacitance with respect to gate Voltage for GaNFinFET and Si-FinFET using 10 and 12-nm Channel Widths

Gate Voltage(V)	Gate Capacitance(fF)	Gate Capacitance (fF)	Gate Capacitance (fF)	Gate Capacitance (fF)
	Gate Capacitance of 10 nm Channel Width of GaNFinFET	Gate Capacitance of 10 nm Channel Width of Si-FinFET	Gate Capacitance of 12 nm Channel Width of GaNFinFET	Gate Capacitance of 12 nm Channel Width of Si-FinFET
0	0	0	0	0
0.2	2.94356	2.01433	2.5674	1.9543
0.4	5.87653	3.54201	3.9052	3.3245
0.6	6.78593	5.78201	5.8763	5.2341
0.8	8.94568	7.41085	7.8794	7.1453
1	10.12349	9.9823	9.9345	9.5523

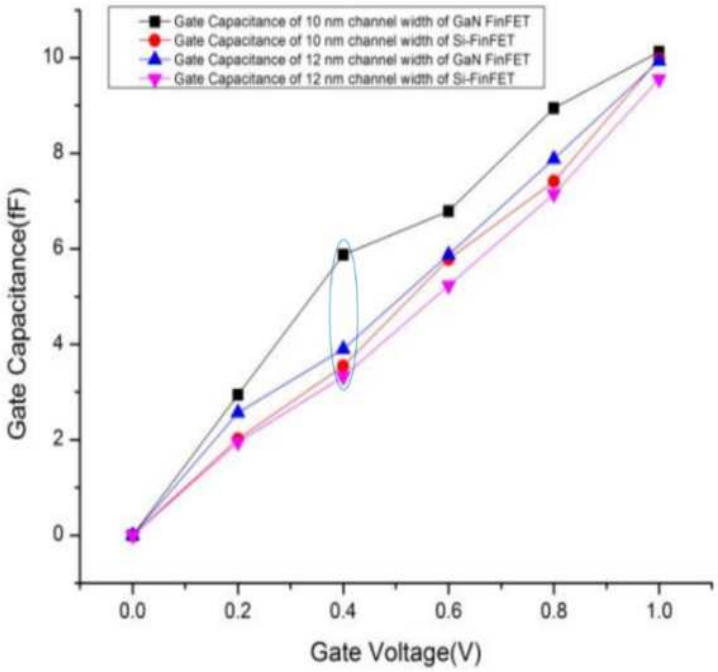

Figure 7: Comparison of Gate Capacitance between GaNFinFET and Si-FinFET using 10 and 12-nm Channels.

In figure 7, we have examined that at the same gate voltage (0.4V), gate capacitance is increased when channel width is decreased from 12 nm to 10 nm for both GaN FinFET and Si-FinFET. It is also observed that gate capacitance as well as leakage current is increased more for 10-nm channel width of GaN FinFET rather than 10-nm channel width of Si-FinFET. From this valuable observation, the electrical property of gate capacitance for Si-FinFET with respect to channel width is better than GaN FinFET transistor.

4.2.2 Comparison of Mobility between GaNFinFET and Si-FinFET using 10 and 12-nm Channel Widths

Table 6: Variation of Mobility with respect to Drain Voltage for GaNFinFET and Si-FinFET using 12 and 10-nm channel Widths

Drain Voltage(V)	Mobility(cm^2/Vs)	Mobility(cm^2/Vs)	Mobility(cm^2/Vs)	Mobility(cm^2/Vs)
	Mobility of 10 nm channel Length of GaNFinFET	Mobility of 10 nm channel length of Si-FinFET	Mobility of 12 nm channel Length of Si-FinFET	Mobility of 12 nm channel Length of GaNFinFET
0	0	0	0	0
0.2	9.1234E-11	8.3871E-11	9.2345E-12	8.5E-11
0.4	1.13524E-10	1.0021E-10	1.3428E-11	1.12E-10
0.6	1.2543E-10	1.12654E-10	1.4325E-11	1.234E-10
0.8	1.37124E-10	1.31093E-10	1.5437E-11	1.353E-10
1	1.45623E-10	1.4012E-10	1.5903E-11	1.4311E-10
1.2	1.53241E-10	1.48265E-10	1.621E-11	1.5123E-10

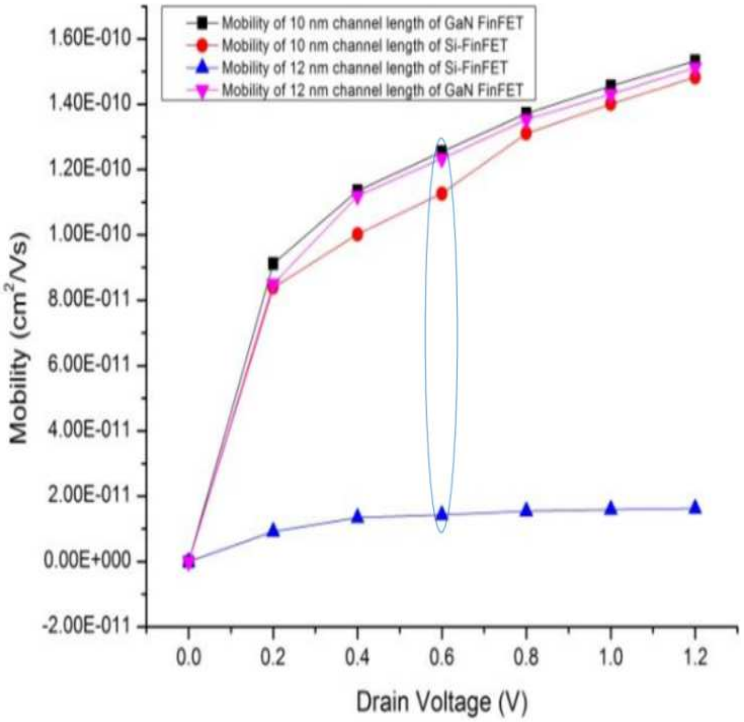

Figure 8: Comparison of Mobility between GaNFinFET and Si-FinFET using 10 and 12-nm channel widths.

In the depicted figure 8, we have shown that if we increase the drain voltage, mobility for both Si-FinFET and GaN FinFET, increases. Moreover, at the same drain voltage, (0.4 V) mobility is increased more when channel width is decreased from 12 nm to 10 nm for both GaN FinFET and Si-FinFET. It is also shown that mobility as well as electron drift velocity is increased more for 10-nm channel width of GaN FinFET rather than 10-nm channel width of Si-FinFET. From this observation point of view, we have decided that more reduced channel width of GaN FinFET is better than Si-FinFET.

4.2.3 Comparison of Gate DIBL between GaNFinFET and Si-FinFET using 10 and 12-nm Channel Widths

Table 7: Variation of DIBL with respect to Gata Voltage for GaNFinFET and Si-FinFET using 10 and 12-nm channel Widths

Gate Voltage(V)	DIBL(mV/V)	DIBL(mV/V)	DIBL(mV/V)	DIBL(mV/V)
	DIBL of 10 nm Channel Width of GaNFinFET	DIBL of 10 nm Channel Width of Si-FinFET	DIBL of 12 nm Channel Width of GaNFinFET	DIBL of 12 nm Channel Width of Si-FinFET
0	0.11231	0.14236	0.15467	0.17654
0.2	0.13245	0.16431	0.16784	0.18564
0.4	0.15713	0.17316	0.17543	0.19765
0.6	0.17351	0.18256	0.18465	0.21543
0.8	0.18452	0.18921	0.19127	0.24325
1	0.19564	0.19561	0.19886	0.27296

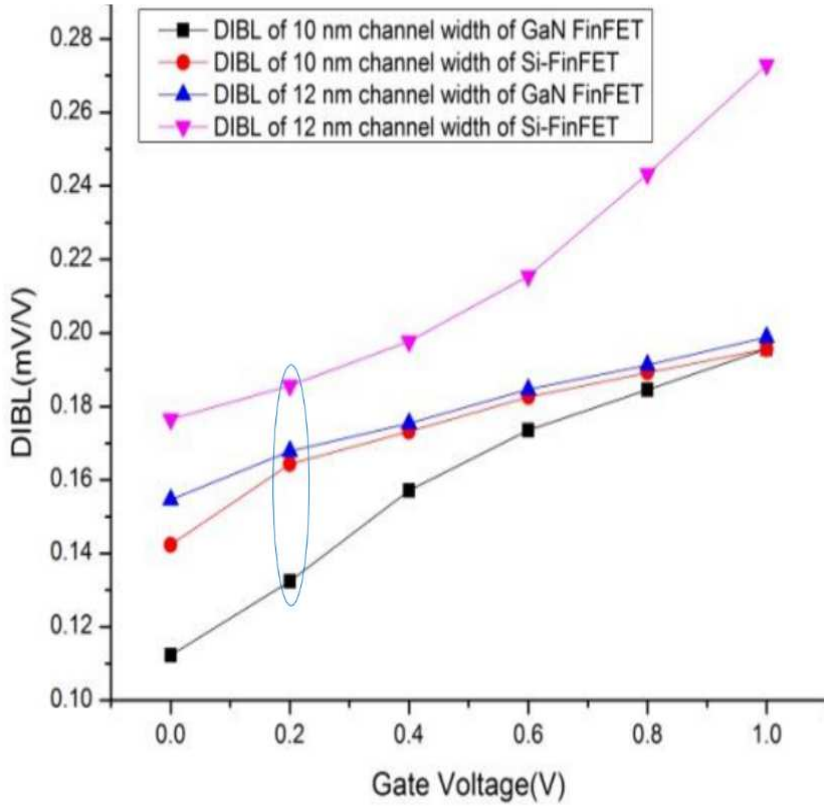

Figure 9: Comparison of Gate DIBL between GaNFinFET and Si-FinFET using 10 and 12-nm channel Widths.

In figure 9, we have presented that if we increase the gate voltage, DIBL for both Si-FinFET and GaN FinFET increases. Moreover, at the same gate voltage (0.4V), DIBL is decreased more when channel width is decreased from 12 nm to 10 nm for both GaN FinFET and Si-FinFET. It is also observed that DIBL is decreased more for 10-nm channel width of GaN FinFET rather than 10-nm channel width of Si-FinFET. From this observation, we have considered that a more reduced channel width of GaN FinFET is better than Si-FinFET to design high-performance nanometer scale FinFETs.

4.2.4 Comparison of Gate Work Function between GaNFinFET and Si-FinFET using 10 and 12-nm channel Width

Table 8: Variation of Gate Work Function with respect to gate length for GaNFinFET and Si-FinFET using 8 and 10-nm Channel Widths

Gate Length(μm)	Work Function(eV)	Work Function(eV)	Work Function(eV)	Work Function(eV)
	Work Function of 12 nm Channel Width of GaNFinFET	Work Function of 12 nm Channel Width of Si-FinFET	Work Function of 10 nm Channel width of Si-FinFET	Work Function of 10 nm Channel Width of GaNFinFET
0	1.12432	1.0131	1.1	1.14532
0.02	1.15643	1.01152	1.13278	1.17812
0.04	1.19721	1.01232	1.1721	1.21563
0.06	1.24317	1.01345	1.193	1.26981
0.08	1.30521	1.0458	1.27234	1.32621
0.1	1.41356	1.1142	1.3251	1.4391

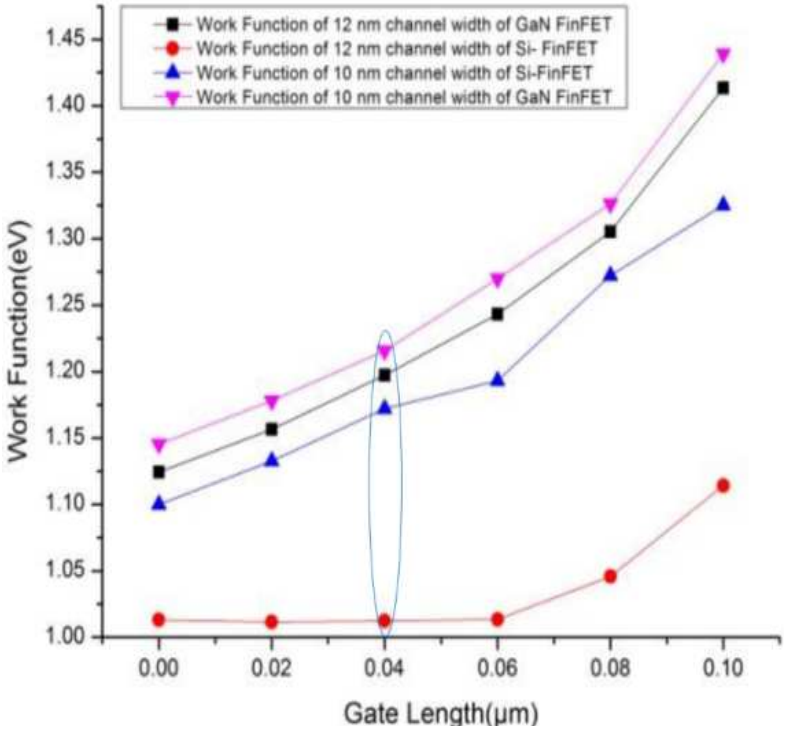

Figure 10: Comparison of gate work function between GaNFinFET and Si-FinFET using 10 and 12-nm Channel Widths.

In figure 10, we have noticed that if we increase the gate length, GWF for both Si-FinFET and GaN FinFET increases. Further, at the same gate length (0.02 μm) GWF is increased when channel width is decreased from 12 nm to 10 nm for both GaN FinFET and Si-FinFET. It is also observed that GWF is increased more for 10-nm channel width of GaN FinFET rather than 10-nm channel width of Si-FinFET. From this valuable observation, we have mentioned that the electrical property of GWF for Si-FinFET is better than GaN FinFET transistor.

4.3 Impacts of Variations of Gate Work Function

4.3.1 Comparison of Threshold Voltage between GaN FinFET and Si-FinFET using 8 and 10-nm Gate Length

Table 9: Variation of Threshold Voltage with respect to GateWork Function for GaN FinFET and Si-FinFET using 8 and 10-nm GateLength

Gate Work Function (eV)	Threshold Voltage(V)	Threshold Voltage(V)	Threshold Voltage(V)	Threshold Voltage(V)
	Threshold Voltage of 8 nm Gate Length of GaNFinFET	Threshold Voltage of 8 nm Gate Length of Si-FinFET	Threshold Voltage of 10 nm Gate Length of GaNFinFET	Threshold Voltage of 10 nm Gate Length of Si-FinFET
0	0.1548	0.18923	0.19678	0.2
0.2	0.21546	0.2433	0.29109	0.3165
0.4	0.32426	0.36213	0.36345	0.4
0.6	0.41428	0.43892	0.48123	0.514
0.8	0.56341	0.59123	0.61562	0.64183
1	0.63216	0.67123	0.72351	0.75324

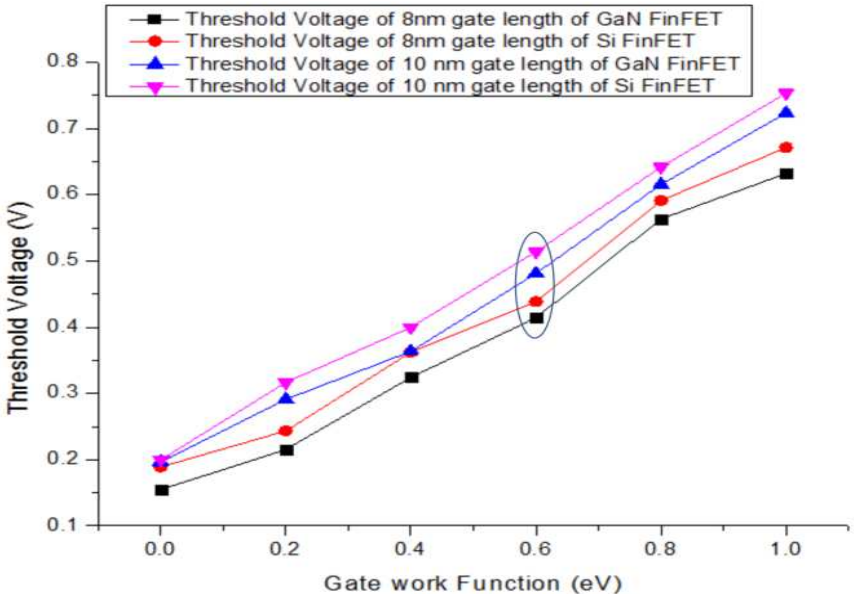

Figure 11: Comparison of Threshold Voltage between GaN FinFET and Si-FinFET using 8and 10 nm Gate Length.

The threshold voltage is a very important parameter for obtaining a higher on-state current, which improves the circuit speed. As the threshold voltage decreases, the on-state current as well as drain current increases. For this reason, the average velocity of the electrons flowing from source to drain will be increased at a given gate voltage. If the threshold voltage is increased, more gate voltage is required for transistor to go on an on-state mode. So, the relatively lower threshold voltage is considered to design a robust nanoscale FinFET device. In figure 11, we have presented that if we increase the gate work function, threshold voltage for both Si-FinFET and GaN FinFET increases. Moreover, at the same gate work function (0.6ev), threshold voltage is decreased more when gate length is decreased from 10 nm to 8 nm for both GaN FinFET and Si-FinFET. It is also observed that threshold voltage is decreased more for 8-nm gate length of GaN FinFET rather than 8-nm gate length of Si-FinFET. From this observation, we have considered that a more reduced gate length of GaN FinFET is better than Si-FinFET to design an efficient nanoscale FinFET device.

4.4 Limitations

The increased gate capacitance and gate work function are observed for both 8-nm channel length and 10-nm channel width of GaN FinFET rather than same size of Si-FinFET. Reduction of gate length involves serious short channel effects in nanodevices. The degrading performances of electrical parameters of GaN and Si-FinFETs and abnormal results have been shown the simulator by using the channel length as well as gate length less than 8 nm. In this paper, we have used only dual gate, 2D device model for proper simulation results.

5. CONCLUSIONS

We have examined that GaN is the better III–V compound material-based channel than conventional Si channel for comparing several electrical parameters. In this paper, we have carefully observed the impact of variations of channel lengths (8 and 10 nm), gate lengths (8 and 10 nm) and channel widths (10 and 12 nm) on electrical parameters such as mobility, DIBL, threshold voltage, gate capacitance and gate work function of double gate n-channel GaN FinFET and Si-FinFET. We have noted that mobility as well as electron drift velocity at the same drain voltage is increased more for both 8- channel length and 10-nm channel widths of GaN FinFET rather than same size of Si-FinFET. Almost always, higher

mobility leads to better electrical potential, conductivity and transconductance. As a result, more drain current (on current) is generated from the device. We have displayed that at the same-gate voltage DIBL is decreased more for both 8-nm channel length and 10-nm channel width of GaN FinFET rather than same size of Si-FinFET. For low power nanodevices, lower DIBL is considerable. The reduced DIBL can improve threshold voltage roll-off property, maintained properly device operating frequency and also minimized SCE. We have observed that the same gate work function threshold voltage is decreased more when gate length is decreased from 10 nm to 8 nm for GaN FinFET than Si-FinFET. As the threshold voltage decreases, the on-state current as well as drain current increases. For this reason, the average velocity of the electrons flowing from source to drain will be increased at a given gate voltage. From the above-mentioned observations, we have considered that a more reduced channel length, width and gate length of GaN FinFET is better than Si-FinFET for electrical parameters, such as mobility, DIBL and threshold voltage to design an efficient nanoscale FinFET device.

We have shown that at the same gate, voltage gate capacitance is increased more for both 8-- channel length and 10-nm channel widths of GaN FinFET rather than same size of Si-FinFET. The gate capacitance is strongly dependent on threshold voltage. Higher the gate capacitance, lesser the threshold voltage. As the threshold voltage decreases, leakage current increases. We have presented at the same gate length, Gate Work Function (GWF) is increased more for both 8-nm channel length and 10-nm channel width of GaN FinFET rather than same size of Si-FinFET. The GWF is the minimum energy needed to remove an electron immediately from solid surface to the outside of the solid surface. The GWF modulates energy bands of semiconductor devices. Higher GWF bends energy band upwards and increases threshold voltage, but on current, transconductance as well as conductivity will be decreased. As a consequence, lower GWF is required for n-channel FinFETs. From the above-mentioned observations, we have considered that more reduced channel length, width of Si-FinFET is better than GaN FinFET for electrical parameters such as gate capacitance and GWF.

In future, the observed limitations of this research work will be successively solved by using trigate or gate all around, 3D FinFET device model.

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